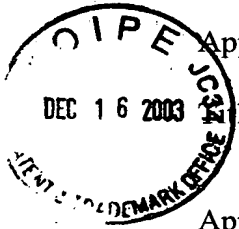


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant: Tomoharu TANAKA et al.

Title: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE
AND MEMORY SYSTEM USING THE SAME

Appl. No.: 09/722,474

Filing Date: 12/28/2000

Examiner: V. Le

Art Unit: 2824

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Mail Stop PATENT APPLICATION
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), within three (3) months of the filing date of the application.

RELEVANCE OF EACH DOCUMENT

All of the documents are either in English or English translations have been provided herewith.

The documents being submitted have been identified in relevant filings from an on-going litigation involving certain parent patents to the current application, which parent patents are U.S. Patents No. 5,546,351, No. 5,724,300, 5,793,696. The case caption for the litigation is "Toshiba Corporation v. Lexar Media, Inc." Case No. C 03-00167 CRB, in the Northern District of California.

Two filings from the *Lexar* litigation are being submitted herewith, which identify the other relevant documents for submission (see References A23 and A24). These filings also outline allegations made by Lexar of invalidity of the parent patents and inequitable conduct related to the parent patents. Documents cited in the filing but not submitted herewith have been previously submitted in the current application. The examiner is welcome to consider all references cited herein or previously cited.

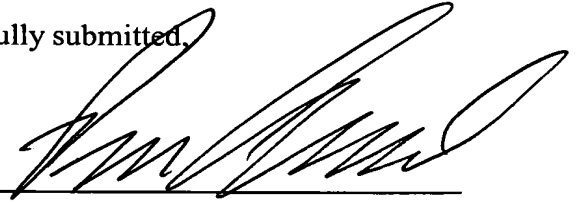
Should the examiner wish to have any further information regarding the litigation, the examiner is welcomed to contact the undersigned.

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

By



Date December 16, 2003

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Attorney for Applicant

Registration No. 40,888

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Date Submitted: December 16, 2003

Use as many sheets as necessary)

2 of 2

Complete if Known

Application Number	09/722,474
Filing Date	12/28/2000
First Named Inventor	Tomoharu TANAKA
Group Art Unit	2824
Examiner Name	V. Le
Attorney Docket Number	016887-1026

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A19	M. Momodomi et al., "A High Density NAND EEPROM with Block-Page Programming for Microcomputer Applications", Proceedings of the IEEE 1989 Custom Integrated Circuits Conference, May 15-18, 1989, pages 10.1.1-10.1.4.	
	A20	T. Tanaka, et al., "A Quick Intelligent Program Architecture for 3V-only NAND-EEPROMs", 1992 Symposium on VLSI Circuits, Digest of Technical Papers, pages 20-21.	
	A21	M. Asakura et al., "An Experimental 1-Mbit Cache DRAM with ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 5-10.	
	A22	R. Vancu et al., "Section 4: Nonvolatile and Fast Static Memories: A 35 ns 256k CMOS EEPROM with Error Correcting Circuitry", 1990 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Feb. 1990, pages 64-65	
	A23	Lexar Media, Inc.'s Corrected Answer to Toshiba corporation's Amended Complaint for Patent Infringement, Case No. C03-00167 CRB, March 5, 2003, pages 1-13.	
	A24	Lexar Media's Amended Patent Local Rules 3-3 and 3-4 Disclosures, Case No. C03-00167, October 16, 2003, pages 1-33 with Exhibits A-I.	
	A25	C.L. Chen et al., "Error-Correcting Codes for Semiconductor memory Applications: A State-of-the-Art Review", IBM J. Res. Develop., Vol. 28, No. 2, March 1984, pages 124-134.	

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under: WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Date Submitted: December 16, 2003

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Sheet 1 of 2

Complete if Known

Application Number	09/722,474
Filing Date	12/28/2000
First Named Inventor	Tomoharu TANAKA
Group Art Unit	2824
Examiner Name	V. Le
Attorney Docket Number	016887-1026

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A1	4,794,564		WATANABE	12-27-1988	
	A2	5,297,096		TERADA ET AL.	03-22-1994	
	A3	5,357,462		TANAKA ET AL.	10-18-1994	
	A4	5,379,256		TANAKA ET AL.	01-03-1995	
	A5	5,544,117		NAKAYAMA ET AL.	08-06-1996	
	A6	3,917,933		SCHEUNEMAN ET AL.	11-04-1975	
	A7	4,456,995		RYAN	06-26-1984	
	A8	4,937,830		KAWASHIMA ET AL.	06-26-1990	
	A9	4,958,352		NOGUCHI ET AL.	09-18-1990	
	A10	5,452,311		WELLS ET AL.	09-19-1995	
	A11	4,980,888		BRUCE ET AL.	12-25-1990	
	A12	5,657,270		OHUCHI ET AL.	08-12-1997	
	A13	5,436,913		YAMAMURA ET AL.	07-25-1995	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	A14	JP	59-110096	A	MITSUBISHI ELECTRIC CORP.	06-25-1984		Transl.
	A15	JP	2-142000	A	HITACHI CORP. ET AL.	05-31-1990		Transl.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A16	K. Arimoto et al., "A Speed-Enhanced DRAM Array Architecture with Embedded ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 11-17.	
	A17	K. Kobayashi et al., "A High-Speed Parallel Sensing Architecture for Multi-Megabit Flash E ² PROM's", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 79-83.	
	A18	M. Momodomi et al., "An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, Oct. 1989, pages 1238-1243.	

Examiner Signature

Date Considered

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